

What is claimed is:

- 1           1.     A digital signal processing circuit comprising:  
2           a chain of processing units to receive indications of discrete input values, each processing  
3     unit being associated with one of a group of filter coefficients; and  
4           a tap selection circuit to select a group of the processing units of the chain to produce an  
5     indication of a filtered discrete output value for each discrete input value.

- 1 *Sub* 2.     The processing unit of claim 1, wherein the chain of processing units comprises a  
*B1* 2     systolic chain.

- 1           3.     The processing circuit of claim 1, wherein the tap selection circuit selects a  
2     number of taps of the processing circuit.

- 1           4.     The processing circuit of claim 1, wherein the group of processing units  
2     progressively accumulate a summed value to form each output value and the tap selection circuit  
3     comprises:  
4     a multiplexer to designate a point in the chain at which the accumulation begins.

- 1 *Sub* 5.     The processing circuit of claim 4, wherein each processing circuit comprises a  
*B2* 2     first input terminal to receive the indications of the discrete input values from a processing circuit  
3     input line common to the processing circuits and a second input terminal to receive the  
4     indications of the discrete input values from another processing circuit, the multiplexer coupling  
5     the first and second terminals of one of the processing circuits together to designate the point in  
6     the chain at which the accumulation begins.

*Sub B2*

1 6. The processing circuit of claim 1, wherein each processing circuit comprises:  
 2 a first adder circuit to generate an indication of a summation of two of the discrete input  
 3 values; and  
 4 a multiplier circuit coupled to the first adder circuit to generate an indication of a product  
 5 of a coefficient associated with said each processing circuit and the summation of the two  
 6 discrete values.

1 7. The processing circuit of claim 6, further comprising:  
 2 a second adder circuit coupled to the first multiplier circuit to combine the summation of  
 3 the two discrete input values with a progressive summation provided by another processing  
 4 circuit.

1 8. The processing circuit of claim 7, wherein the tap selection circuit comprises:  
 2 a multiplexer to selectively furnish an indication of a zero to the second adder circuit of  
 3 one of the processing units to designate a point where the progressive sum begins.

1 9. The processing circuit of claim 1, wherein the tap selection circuit comprises:  
 2 a register storing bits indicative of the processing units in the group.

1 10. The processing circuit of claim 1, wherein each processing unit comprises:  
 2 a register storing the indication of the associated filter coefficient.

*Sub B3*

1 11. The processing circuit of claim 1, wherein the processing circuit comprises a  
 2 finite impulse response filter.

1 12. The processing circuit of claim 1, wherein the processing circuit comprises an  
 2 infinite impulse response filter.



